HARDWARE

REFERENCE DESIGN

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UFirebird-UC6226 (QFN40)

GNSS Positioning Chip

Revision History

Version	Revision History	Date
Ver. 1.0	HW reference design, Primary	Aug. 2018
Ver. 1.3.1	Delete the second solution in chapter antenna detection; DCDC Bypass reference design, add two 1uF decoupling capacitors to the input end of main supply; 1 uF decoupling capacitor at the output end of LDO_X_OUT and input end of TCXO supply; Revise the description of the anti-series resistance section.	Aug. 2019
R1.4	Fix the problem of typo in chapter 2.1 Power and 2.2 RTC	2019-09-11
R1.5	Update Copyright time	2020-04-13
R1.6	Update the notes in schematics.	2020-05-06
R1.7	Update the range of IO supply; Update notes and attentions; Add the requirement for RTC pins when hot start function is not used	2021-10-25
R1.8	Update the parameters of VDD_IO and the reference design of antenna detection	2022-03-24
R1.9	When RTC is not used, the RTC_O pin should be grounded and RTC_I be floating.	2022-11-16
R1.10	Optimize the description of antenna power supply; Add recommended BOM	Apr. 2023

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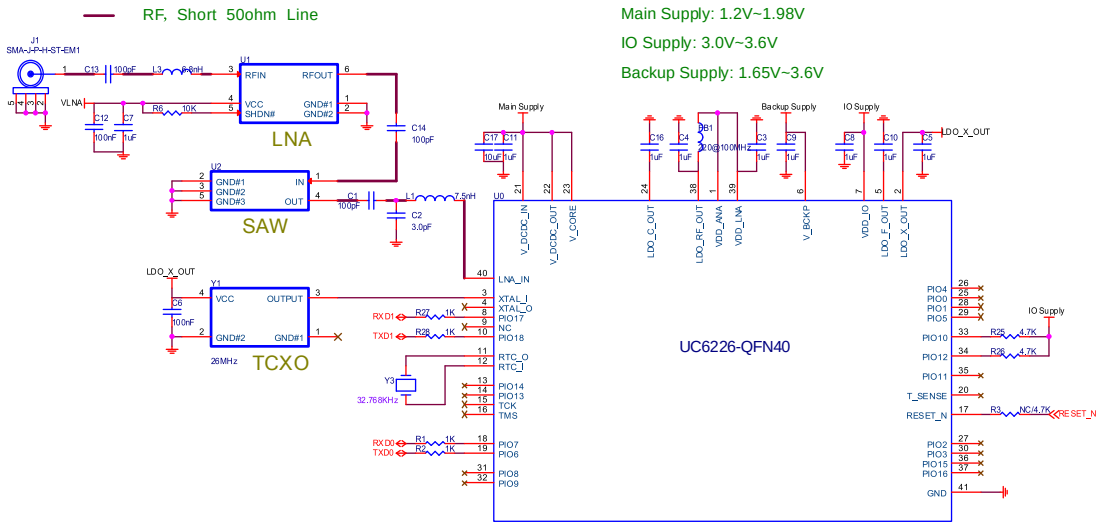
Contents

1 Reference Design

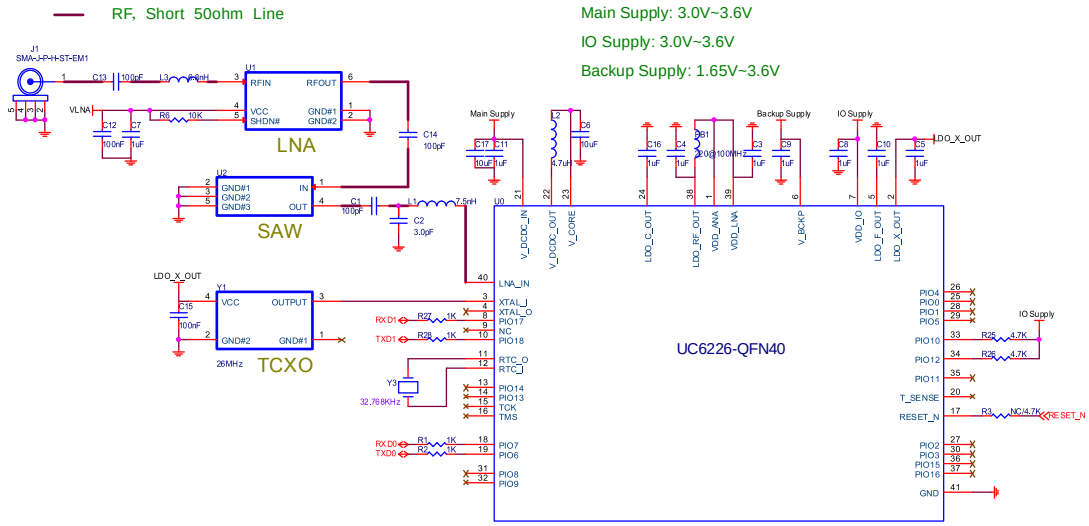
1.1 High-performance Solution

- DCDC bypass
- External LNA
- RTC Crystal
- UART interface



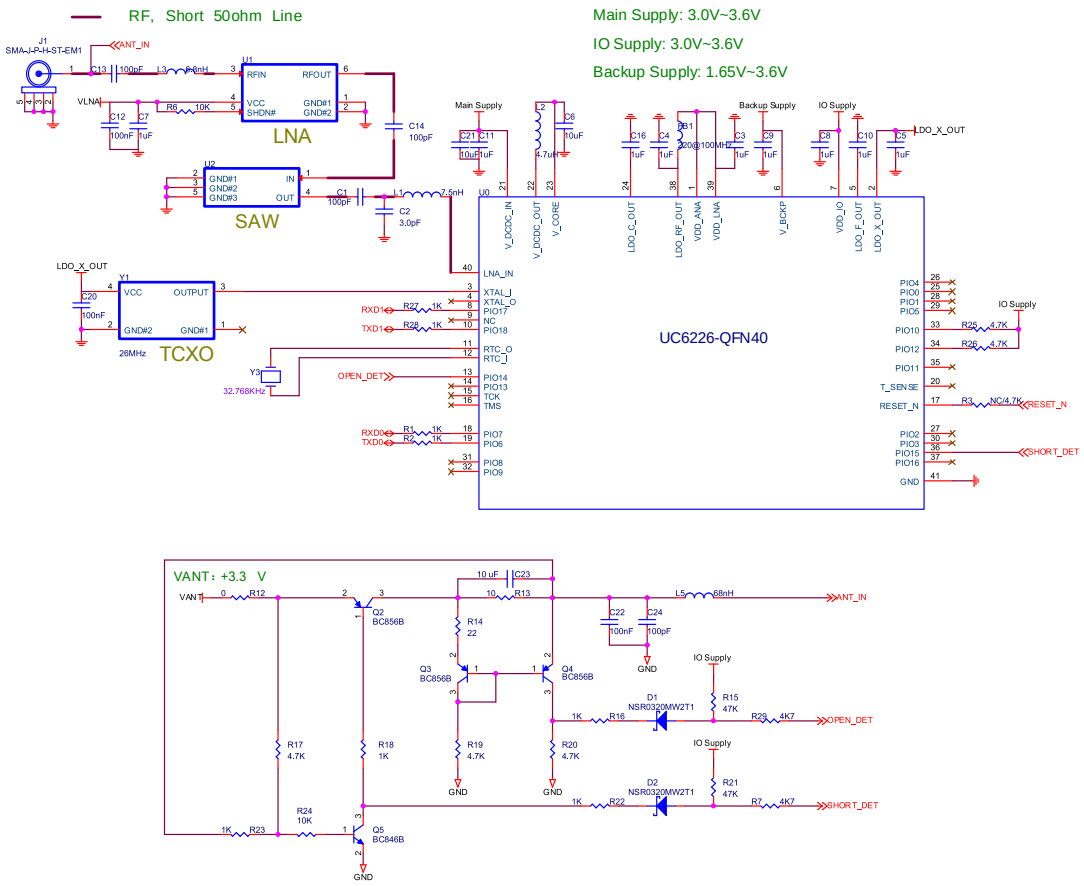
1.2 Low Power Scheme

- Use Internal DC/DC
- RTC Crystal
- UART interface



Note: The L2 inductance at V_DCDC_OUT is required to be 4.7 uH.

1.3 Antenna Detection



Antenna State	OPEN_DET	SHORT_DET
Open circuit	1	0
Short circuit	0	1
Normal	0	0

In the figure above, “VANT” is a standard +3.3 V power supply which feeds the antenna through a 68 nH inductor L5 at the upper right. When designing PCB layout, the distance between the inductor L5 and the node that connects ANT_IN and the RF line should be as short as possible—it is recommended to place one of the metal pads of the L5 inductor on the RF line. “OPEN_DET” and “SHORT_DET” are status indicators of the antenna.

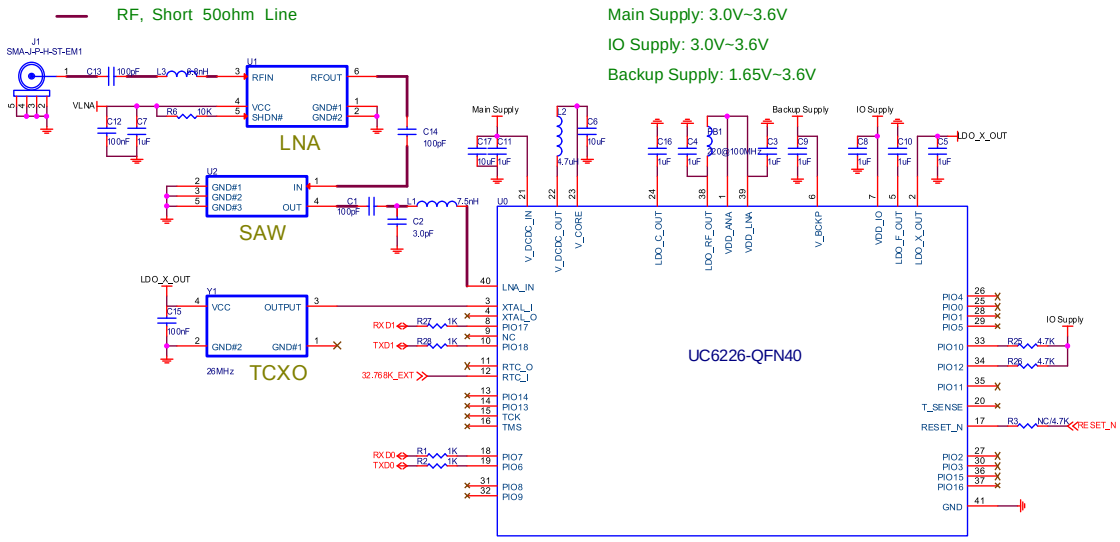
☞ When designing circuits, please note that the antenna power supply voltage should be +3.3V, and the current should not exceed 80mA. If the voltage or current is beyond that range, the circuit parameters need to be adjusted to ensure that SHORT_DET and OPEN_DET signals match the state values in the above table.

☞ If the antenna power supply and the chip's main supply use the same power rail, the ESD, surge and overvoltage from the antenna will have an effect on the main supply, which may cause damage to the chip. Therefore, it's recommended to design an independent power rail for the antenna to reduce the possibility of damage to the chip.

Note: The L2 inductance at V_DCDC_OUT is required to be 4.7 uH.

1.4 RTC without Crystal

- RTC 32.768 kHz is provided by an external clock
- The high level of the external clock signal must be less than 1.05 V



Note: The L2 inductance at V_DCDC_OUT is required to be 4.7 uH.

2 Attention

2.1 Power

V_DCDC_IN and VDD_IO power supply are independent of each other. If the two power supply voltages are different, a separate external power supply is required. If the two sources have the same voltage, they can be supplied from the same external source.

There is no strict sequence requirement for V_DCDC_IN and VDD_IO, but the lack of any one of them would keep the chip in reset state. The rise time of V_DCDC_IN and VDD_IO when power on should be less than 10 ms and the power supply should be monotonic. After UC6226 is powered on, the start-up time should be more than 230 ms, otherwise the chip may work abnormally.

Note: when the VDDIO and V_DCDC_IN/V_CORE adopt the same source power supply, the signal status of host ports communicating with the chip UART needs to be clarified. When the host computer wants to control the power loss of the chip, the ports connected with the chip should be set at high resistance state to prevent the chip from consuming the power of the host computer even after the shutdown. PIO7 and PIO6 need concatenate 1 KΩ resistance, if the rest of the PIOs are needed, such as Reset, antenna, recommending to concatenate resistance which is at the range of 1 KΩ to 4.7 KΩ (set the resistance value according to the number of ports connected, use 1 KΩ for a small number of ports, and increase the resistance value appropriately for more ports, the maximum value is 4.7 KΩ).

V_BCKP is backup power, if the application requires support hot start function. It needs to be powered independently.

2.2 RTC

RTC is usually driven by 32.768 kHz oscillator, which needs to connect external 32.768 kHz crystal.

If GNSS hot start function is not needed, RTC crystal can be omitted. Under this condition, RTC_O should be grounded, and RTC_I should be floating.

UC6226 also supports external 32.768 kHz digital clock signal directly input RTC_I pin to replace the crystal. When using external digital clock signal input RTC_I, be sure that the high level of the signal must be less than 1.05 V, or it may lead to UC6226 getting burned.

Level requirement for the input signal: high level 0.9 V~1.05 V, low level 0 V~0.2 V.

Waveform requirement for the clock: duty cycle range should be 45% ~ 55%, clock error range should be ±0.6 Hz, ±20 ppm.

RTC layout and routing should follow the general rules of RTC layout and routing, with special attention to:

1) Use a proper GND concept ;
2) The RTC crystal shall be placed as close to the chip as possible, and there shall be no other devices between the two;
3) Devices, signals, wiring, etc. with high power or strong interference should be avoided around RTC crystal;
4) It is recommended to ground shield with the relevant circuits of RTC.

2.3 TCXO

The CLK_I pin is used for connecting an external TCXO of 26 MHz. The power supply of TCXO can be LDO_X or an external independent power supply.

The basic parameter requirements for TCXO are as follows:

1. Frequency and temperature: 26 MHz ± 0.5 ppm (-40 °C ~ +85 °C)
2. Short-term frequency stability: <10 ppb
3. Output voltage range: -0.2 V ~ 1.05 V
4. Output peak-to-peak voltage Vpp: 0.3 V ~ 1 V

Special attentions should be paid to the layout and routing of TCXO in addition to the general rules:

1. It is recommended to maintain copper void for the layer where TCXO is placed and the adjacent layers, and keep the reference ground complete for other layers, so as to reduce the impact of heat conduction on the performance of TCXO.
2. Place the TCXO away from any heat source or interference source, with ground shields for the surrounding circuits.
3. Avoid placing any high-power or strong interference devices, signals, traces, etc. around the TCXO. Keep a distance of more than 3 times the trace width between the clock signal trace and other signal traces.

3 Recommended BOM

Component	Manufacturer	Order No.
LNA	MAXSCEND	MXDLN16GF
	MAXIM	MAX2659ELT+T
SAW	TAI-SAW	TA0757A; TA1661A
TCXO	EPSON	X1G003841003400
	KDS	1XXD26000MAA

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